

## PLATING METHOD FOR PCB

### BACKGROUND OF THE INVENTION

#### 5           1.       Field of the Invention

The present invention relates to a printed circuit board and, more particularly, to a plating method for a printed circuit board that is capable of forming a plated layer without a power supply line for gold-plating at a pad.

#### 10           2.       Description of the Background Art

Figure 1 is a plane view showing a major part of a printed circuit board in accordance with a conventional art, and Figure 2 is a sectional view showing the major part of a printed circuit board in accordance with the conventional art.

As shown in Figures 1 and 2, a plurality of printed circuit boards 1a and 1b  
15 are formed on one substrate 1 and as they are separated, the plurality of printed circuit boards 1a and 1b are completely produced.

In the conventional printed circuit board, there are formed at a surface of a base material 8, a plurality of bonding pads 3 on which a plurality of bonding wires are bonded to be electrically connected to a semiconductor chip and a plurality of  
20 ball pads 4 on which a solder ball is attached for connection with another printed circuit board. And circuit patterns are formed by a single layer or multi-layer inside the printed circuit board. The bonding pads 3 and the ball pads 4 are electrically connected to the circuit patterns.

The bonding pad 3 and the ball pad 4 are gold-plated to heighten a bond  
25 strength with a gold wire and solder ball. A power supply line 5 and a plurality of

lead-in wires are formed on the surface of the printed circuit board for supplying power to the bonding pad 3 and ball pad 4, thus to gold-plate on the pad 3 and 4.

The power supply line 5 is formed long with a certain width at the center of the surface of the base material 8, and the lead-in wires 6 are branched from the power supply line 5 and connected to the bonding pads 3 or the ball pads 4. Because much current flows in the power supply line 5, the power supply line 5 is formed wider in its width than the lead-line wires 6.

In the printed circuit board of the conventional art, when power is supplied to the power supply line 5 from an external source, power is supplied to the bonding pads 3 and the ball pads 4 through the plurality of lead-in wires 6, performing a gold-plating.

When the gold-plating process is completed, a process is performed to separate to a plurality of printed circuit boards. That is, cutting along a router cut line 7 by using a router separates printed circuit boards 1a and 1b.

At this time, because the router cut line 7 is wider than the power supply line 5, when the printed circuit boards 1a and 1b are separated, the power supply line 5 is removed so that each bonding pad 3 and ball pad 4 is electrically short and only the lead-in wires 6 remain.

However, the plating method for the printed circuit board in accordance with the conventional has the following problems.

That is, because the lead-in wires 6 to which the bonding pads and ball pads 4 are connected remain at the surface of the completed printed circuit boards 1a and 1b, when a semiconductor chip is mounted for use on the printed circuit board, the lead-in wires 6 cause an interference with peripheral circuits or increase a power consumption and serve as an element hindering a signal flow,

resulting in degradation of a performance of a product.

In order to solve the problems, as shown in Figure 3, the lead-in wires are removed by etching method after performing a gold-plating on the bonding pads 3 and the ball pads 4.

5 In this case, however, it is difficult to accurately deposit an etching resist only at the region of the bonding pad 3 and the ball pad 4. Also, another problem arises that when the lead-in wires are removed, an etching solution is bound to infiltrate into the bonding pads 3 and the ball pads 4, removing even the bonding pad 3 and the ball pad 4. Thus, in order to avoid such a problem, the lead-in wire 6  
10 is not completely removed, leaving a residual lead-in wire.

Even in this case, however, existence of the residual lead-in wire 10 causes the same problem as described above, more or less.

In addition, in the printed circuit board of the conventional art, it is difficult to process the solder resist because the lead-in wires are removed after the circuit  
15 process.

## SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a plating method  
20 for a printed circuit board that is capable of reducing power consumption and improving a performance of a product by providing a printed circuit board with a lead-in wire.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described herein,  
25 there is provided a plating method for a printed circuit board including: A plating

method for a printed circuit board comprising: a first step of providing a substrate having a plurality of connection pads and circuit patterns connected to the connection pads; a second step of using some of the circuit patterns provided on a surface of the substrate as a power connection portion and connecting the power connection portion to an external power source; a third step of covering a surface of the substrate excepting the connection pads with a plating resistance resist to shield it; a fourth step of supplying power to the connection pad through the power connection portion and forming a gold-plated layer on the connection pad; and a fifth step of making the power connection portion and the external power source to be electrically short.

In the plating method for a printed circuit board of the present invention, the second step includes: coating a photoresist at the surface of the substrate; removing a portion of the photoresist to expose the connection pad and exposing some of the circuit patterns to form a power connection portion; and coating an electrolyte layer on the surface of the substrate for connecting between the power connection portion and an external power source.

In the plating method for a printed circuit board of the present invention, the electrolyte layer is formed through an electroless plating method, and the electrolyte layer has a thickness of 0.3~0.7 $\mu$ m.

In the plating method for a printed circuit board of the present invention, in the third step, the plating resistance resist is coated at the surface of the substrate with the electrolyte layer formed thereon, and the fifth step includes: removing the electrolyte layer and the plating resistance resist; and coating a photoresist at the surface of the electrolyte layer and the plating resistance resist-removed substrate to cover the power connection portion to make power short.

To achieve the above objects, there is also provided a plating method for a printed circuit board including: a first step of providing a substrate having a plurality of bonding pads and ball pads at both sides thereof and a circuit pattern to which the bonding pads and the ball pads are connected; a second step of using some of the circuit patterns provided at the surface of the substrate as first and second power connection portions and connecting the first power connection portion to an external power source; a third step of covering the surface of the substrate with the ball pad formed thereon with a plating resistance resist to shield it; a fourth step of supplying power to the bonding pad through the first power connection portion to form a gold-plated layer on the bonding pad; a fifth step of making the first power connection portion and the external power source to be electrically short; a sixth step of connecting the second power connection portion to the external power source and coating a plating resistance resist at the surface of the substrate with the ball pad formed thereon to shield it; a seventh step of supplying power to the ball pad through the second power connection portion to form a gold-plated layer on the ball pad; and an eighth step of making the second power connection portion and the external power source to be electrically short.

In the plating method for a printed circuit board of the present invention, the second step includes: coating a photoresist at both surfaces of the substrate; removing a portion of the photoresist to expose the bonding pad and the ball pad and exposing some of the circuit patterns to form first and second connection portion; and coating an electrolyte layer at the surface of the substrate where the ball pad is formed in order to connect the first power connection portion to an external power source.

In the plating method for a printed circuit board of the present invention,

the fifth step includes: removing the electrolyte layer and the plating resistance resist; and coating a photoresist at the surface of the electrolyte layer and the plating resistance resist-removed substrate to cover the first power connection portion to make power short.

5           In the plating method for a printed circuit board of the present invention, the sixth step includes: forming an electrolyte layer at the surface of the substrate where the bonding pad is formed to electrically connect it to the second power connection portion; and coating a plating resistance resist at a surface of the electrolyte layer.

10           In the plating method for a printed circuit board of the present invention, the eighth step includes: removing the plating resistance resist and the electrolyte layer; and covering the second power connection portion with a photoresist to make the second power connection to be short electrically.

          The foregoing and other objects, features, aspects and advantages of the  
15   present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

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          The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

25           In the drawings:

Figure 1 is a plane view showing one example of a printed circuit board in accordance with a conventional art;

Figure 2 is a perspective view showing the printed circuit board in accordance with the conventional art;

5        Figure 3 is a plane view showing another example of a printed circuit board in accordance with the conventional art;

Figures 4A to 4L show sequential process of a method for fabricating a circuit pattern of a printed circuit board in accordance with a preferred embodiment of the present invention; and

10        Figures 5A to 5E are plane views sequentially showing a circuit pattern fabrication process of the printed circuit board in accordance with the preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

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Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

Figures 4A to 4L show sequential process of a method for fabricating a circuit pattern of a printed circuit board in accordance with a preferred embodiment  
20 of the present invention.

A plating method for a printed circuit board of the present invention will now be described with reference to Figures 4A to 4L.

First, a substrate 50 is prepared. The substrate 50 includes an insulation layer 52 formed as at least one or more insulation materials are thermally  
25 compressed and a plurality of circuit patterns 54 stacked inside the insulation layer

52. A metal layer 56 is formed at both surfaces of the insulation layer 52, and a plurality of through holes 58 are formed to electrically connect the circuit patterns 54 and the metal layers 56 (refer to Figure 4A).

5 The substrate 50 is fabricated through a fabrication process of a general multi-layer printed circuit board in which circuit patterns are formed on a plurality of insulation plates, which are stacked by plural ones and thermally compressed.

A metal-plated layer 60 is formed at the surface of the substrate 50 through a plating process. The metal-plated layer 60 is formed at the surface of the metal layer 56 and at an inner wall of the through hole 58.

10 The metal-plated layer 60 formed at the surface of the metal layer 56 serves to form circuit patterns 54 and the metal-plated layer 60 formed at the inner wall of the through hole 58 serves to electrically connect the circuit patterns in a follow-up process (refer to Figure 4B).

15 Next, the metal layer 56 and the metal-plated layer 60 are selectively removed to form a circuit pattern 62. That is, the circuit patterns 62 are formed at both surfaces of the substrate 50 through a general exposure/development process and an etching process, and some of the circuit patterns 62 are used as a bonding pad 64 electrically connected to a semiconductor chip and some other circuit patterns are used as a ball pad 66 electrically connected to another printed  
20 circuit board. In general, the ball pad 66 is formed at the opposite side of the side where the bonding pad 65 is formed.

The bonding pad 64 is connected to a gold wire for electrical connection with the semiconductor chip mounted at the printed circuit board, and electrically connected to the circuit pattern 62 formed at the through hole 58 by the  
25 connection pattern 68.

A solder ball is attached to the ball pad 66 for connection with a different printed circuit board, and the ball pad 66 is electrically connected to the circuit pattern 62 formed at the through hole 58 by the connection pattern 68.

After the circuit pattern 62, the bonding pad 64 and the ball pad 66 are  
5 formed at the surface of the substrate 50, a photoresist 70 is coated at the surface of the substrate 50. The photoresist 70 is to protect the circuit patterns 62 and is not coated at the connection pads 64 and 66 making the bonding pad 64 and the ball pad 66.

That is, after the photoresist 70 is coated at the entire surface of the  
10 substrate 50, and the photoresist 70 at the portion of the connection pads 64 and 66 is removed through an additional process to expose the connection pads 64 and 66.

First and second power connection portions 72 and 74 are formed to be used as a path for supplying power to the connection pads 64 and 66.

15 The first and second power connection portions 72 and 74 are formed by exposing a portion of the circuit pattern 62 by removing a portion of the photoresist 70. That is, a portion of the circuit pattern 62 formed connected to the through hole 58 is exposed (refer to Figure 4D).

A process of forming a gold-plated layer at the connection pads 64 and 66  
20 will now be described.

First, electrolyte layers 76 and 78 are formed at the both surfaces of the substrate 50 to connect the first and second power connection portions 72 and 74 to an external power source.

The electrolyte layers 76 and 78 are made of copper and formed through  
25 an electroless plating method or sputtering (refer to Figures 4E and 5A).

Formation of the electrolyte layers 76 and 78 through the electroless plating method is to make the electrolyte layer 76 to be formed well also at the surface of the photoresist 70.

The electrolyte layers 76 and 78 are copper-plated through the electroless  
5 plating method and additionally the electrolyte layers 76 and 78 are copper-plated through an electrolytic copper plating method in order to obtain a desired thickness.

The electrolyte layers 76 and 78 are preferably formed as thin as possible so as to be easily removed in a follow-up process. For example, preferably, the  
10 electrolyte layer 76 and 78 having a thickness of  $0.3\mu\text{m}\sim 0.7\mu\text{m}$ .

And then, a masking process is performed with a plating resistance resist 80 on the opposite side of the side where the bonding pad 64 is formed (refer to Figure 4F).

Thereafter, the electrolyte layer 76 of the surface where the bonding pad  
15 64 is formed is removed through an etching method or the like (refer to Figures 4G and 5B). At this time, because the plating resistance resist 80 has been coated at the surface where the ball pad 66 is formed, that is, the opposite side of the bonding pad 64, the electrolyte layer 78 is not removed.

Besides the above-described method, the electrolyte layer 78 may be  
20 formed only at the surface where the ball pad 66 is formed, while the electrolyte layer 76 may not be formed at the surface where the bonding pad 64 is formed.

In this state, when power (P) is supplied from outside through the first power connection portion 72, power is supplied to the bonding pad 64 through the electrolyte layer 78, the circuit pattern 62 formed at the through hole 58 and the  
25 connection pad 68.

And then, a gold-plated layer 82 is formed at the surface of the bonding pad 64 (refer to Figure 4H). The arrow illustrated in Figure 4H indicates a power supply path and the circuit pattern 62 is formed in a ring shape at the surface of the through hole 58 and electrically connects the first power connection portion 72 and the bonding pad 64.

After the gold-plated layer 82 is completely formed at the bonding pad 64, the plating resistance resist 80 and the electrolyte layer 78 formed at the surface where the ball pad 66 is provided are removed. And then, the first power connection portion 72 is covered with the photoresist 70 to make it electrically short (refer to Figures 4I, 5C and 5D).

After the gold-plated layer 82 is formed at the bonding pad 64, a gold-plated layer 92 is formed at the ball pad 66.

First, electrolyte layers 86 and 88 are formed at both surfaces of the above process-completed substrate 50. Then, the second power connection portion 74 and the electrolyte layer 88 are electrically connected.

Next, a plating resistance resist 90 is coated at the surface of the electrolyte layer 88 formed at the side where the bonding pad 64 is provided.

And then, the electrolyte layer 86 coated at the surface where the ball pad 66 is provided is removed through an etching method or the like (refer to Figure 4J).

In this state, external power (P) is applied to the ball pad 66 through the second power connection portion 74 to form a gold-plated layer 92 at the ball pad 66 (refer to Figures 4K and 5E).

The external power (P) is supplied to the electrolyte layer 88 and applied to the ball pad 66 through the second power connection portion 74 connected to

the electrolyte layer 88 and the circuit pattern 62 formed at the through hole 58 and the connection pad 68.

After the gold-plated layer 92 is formed at the ball pad 66, the plating resistance resist 90 and the electrolyte layer 88 are removed and the second  
5 power connection portion 74 is covered with the photoresist 70 so that the second power connection portion 74 can be electrically short.

As so far described, the method for fabricating a circuit pattern of a printed circuit board fabricated through the above-described process has the following advantage.

10 That is, because some circuit patterns are used as power connection portions and the electrolyte layer is formed at the surface of the substrate to transfer an external power to the connection pad through the power connection portion, a lead-in wire for power supply is not necessary, and thus, a power consumption can be reduced and a performance of a product can be improved.

15 As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims,  
20 and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalence of such metes and bounds are therefore intended to be embraced by the appended claims.